## REMARKS/ARGUMENTS

Claims 1-23, 27, and 28 are presently active in this case. Applicant has amended Claims 1, 8, 15, and 21-23, and added Claims 27 and 28. Support for the amendments may be found at least at page 8, lines 29-31 and page 8, line 34-page 9, line 3, page 11, lines 9-18, and page 14, lines 19-22 of the specification and Figs. 5-8. No new matter has been added.

The outstanding Office Action rejects Claims 1-23 under 35 U.S.C. § 102(e) as being anticipated by Dutton, et al. (U.S. Patent No. 6,061,756, herein "Dutton"). Applicant respectfully traverses the rejection.

To establish anticipation of Claims 1-23 under 35 U.S.C. § 102(e), the outstanding Office Action must show that each and every feature recited in Claims 1-23 is either explicitly disclosed or necessarily present in Dutton.[1]

The present invention relates to a technique to enhance data bus utilization. The outstanding Office Action asserts that Dutton discloses each and every element recited in Claim 1. Applicant respectfully disagrees.

Claim 1 recites a data transfer control circuit for carrying out data transfer by using a plurality of bus masters comprising, *inter alia*, a plurality of bus masters configured to send a request signal requesting a use of each of unit data buses and to use the unit data buses requested when a request by means of the request signal is granted; and one bus controller configured to split-control the unit data buses for the plurality of bus masters by giving a grant signal which grants the use of each of the unit data buses in accordance with the request signal, wherein the request signal has an operand comprising a plurality of bits, each of the plurality of bits corresponding to a respective one of the unit data buses, and the bus controller grants the use of each of the unit data buses specified by the bits of the request

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[1] See M.P.E.P. § 2131.

signal.

Dutton does not disclose at least the above-mentioned bus masters feature of Claim 1. The outstanding Office Action cites col. 9, lines 19-25; however, the above-mentioned bus masters feature is not disclosed there. In Dutton, "each device 142-146 coupled to the bus 120 monitors the data traffic being transmitted on all of the data channels which make up the bus 120."[2] "Each device 142-146 determines the availability of each or every data channel."[3] In other words, in Dutton, each device coupled to the bus monitors the data traffic to determine the availability of each data channel. Then, "a first device 142 asserts ownership over a first one or more available data channels out of all possible data channels."[4] On the other hand, the above-mentioned bus masters feature of Claim 1 is configured to send a request to use each of unit data buses and use some or all of the unit data buses when the request is granted. Nowhere does Dutton disclose a plurality of bus masters configured to send a request signal requesting a use of each of unit data buses and to use the unit data buses requested when a request by means of the request signal is granted, as recited in Claim 1, as amended.

Dutton does not disclose the above-mentioned bus controller feature of Claim 1, either. The outstanding Office Action cites col. 10, lines 26-58; however, the above-mentioned bus masters feature is not disclosed there. The outstanding Office appears to allege that reference numeral 222 in Fig. 3 of Dutton reads on the above-mentioned bus controller feature of Claim 1.[5] In Dutton, "the byte slicing logic 176 or unified logic 176/178 for each respective multimedia device 142-146 may also include an arbitration logic

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[2] Col. 9, lines 14-17 of Dutton.
[3] Col. 9, lines 17-18 of Dutton.
[4] Col. 9, lines 19-21 of Dutton.
[5] See Office Action, page 2.

the devices 142-146 monitors traffic on the data channels of the data packed bus 120."[7] "If

the (sending) device 142-146 needs to transfer data . . . , the arbitration logic 222 in a sending

device asserts ownership of the available one or more data channels . . ."[8] In other words, in

Dutton, each of the devices 142-146 has its own arbitration logic 222, and each of the

arbitration logics 222 monitors traffic on the data channels and asserts ownership of the data

channels only for one of the devices 142-146. On the other hand, the above-mentioned bus

controller feature of Claim 1 is configured to control the unit data buses for a plurality of bus

masters. Nowhere does Dutton disclose a bus controller configured to split-control the unit

data buses for the plurality of bus masters, as recited in Claim 1.

Moreover, Dutton does not disclose the above-mentioned request signal feature that

has an operand comprising a plurality of bits, each of the plurality of bits corresponding to a

respective one of the unit data buses, and the above-mentioned bus controller feature that

grants the use of each of the unit data buses specified by the bits of the request signal. The

outstanding Office Action cites col. 10, lines 26-39; however, he above-mentioned request

signal and bus controller features are not disclosed there. In Dutton, "[i]f the (sending)

device 142-146 needs to transfer data . . . , the arbitration logic 222 in a sending device

asserts ownership of the available one or more data channels . . ."[9] However, Dutton is

completely silent as to how the arbitration logic 222 asserts ownership of the available one or

more data channels. Nowhere does Dutton disclose a request signal that has an operand

comprising a plurality of bits, each of the plurality of bits corresponding to a respective one

of the unit data buses, and a bus controller feature that grants the use of each of the unit data

buses specified by the bits of the request signal, as recited in Claim 1.

Accordingly, Applicant respectfully submits that Claim 1 is patentable and the

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[7] Col. 10, lines 26-29 of Dutton.
[8] Col. 10, lines 40-49 of Dutton.
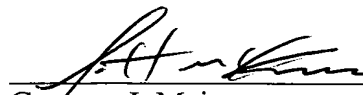[9] Col. 10, lines 40-49 of Dutton.

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rejection of Claim 1 under 35 U.S.C. § 102(e) should be withdrawn. Independent Claims 8, 15, and 21-23, although of different statutory class or of different scope, include recitations similar to those in Claim 1 discussed above. Claims 2-7, 9-14, 16-20, 27, and 28 depend on Claims 1, 8, or 15. For at least the reasons given above with respect to Claim 1, Applicant respectfully submits that Claims 2-23, 27, and 28 are patentable as well.

New Claims 27 and 28 recite the features of Claims 1 and 8, wherein said bus controller send a bus master selection signal to all of said bus masters along with said grant signal, said selection signal indicating a bus master by which said grant signal is to be received. In addition to the reasons discussed above, these claims recite a more detailed aspect of the Applicants invention not shown or suggested by the cited references.

Accordingly, in view of the foregoing amendments and remarks, it is respectfully submitted that the present application, including Claims 1-23, 27, and 28, is patentably distinguished over the prior art, is in condition for allowance, and such action is respectfully requested at an early date.

Respectfully submitted,

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